

sPHENIX tracking simulations

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sPHENIX Cost & Schedule Review
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The tracking options

The tracking options being considered are:

Reused PHENIX pixels		Silicon strip outer tracker
OR	+	OR
MAPS based pixels		TPC outer tracker

The goal of the tracking simulations is to characterize the performance of all of the possible combinations

Outline

- Simulations overview
- Results so far
- Future plans

Overview of silicon tracking simulations

So far the sPHENIX silicon tracking simulations have been done with:

Cylinder cell geometry in G4:

- Make a cylinder, subdivide it into cells (pixel or strip)
- Each cell:
 - Sensor material
 - Cu layer to represent **average** electronics, support, cooling material

Hit finding, clusterizing, tracking, ghost rejection:

- Hough Transform to find tracks
- Kalman Filter to extract track parameters
- Evaluation objects!
- Extensive tuning done for central HIJING events
- Works well
- Next: need realistic ladder geometry model in G4

TPC tracking simulations

So far the sPHENIX TPC **gas** simulations have been done with:

Cylinder cell geometry in G4:

- Make a cylinder of gas,
- subdivide it radially into cells,
 - 45 cells radially, 1 degree in r - Φ
- Drift each voxel to the readout plane
- Diffuse it transversely
- Make a readout plane configuration
- Impose readout parameters to get realistic coverage of pads

Still early days:

- Good estimates of momentum resolution, Upsilon mass resolution
- Lots of work still to characterize tracking performance in AuAu
- Need realistic simulation of space charge effects

Results to date - silicon tracker configuration

Consider the 5 layer silicon tracker configured for the FPHX chip +

- The reused PHENIX pixels
- **OR** a 3 layer MAPS pixel detector (we use $r = 2.4, 4.0, 6.0$ cm here)

Station	Layer	radius (cm)	pitch (μm)	sensor		total thickness $X_0\%$	area (m^2)
				length (cm)	depth (μm)		
Pixel	1	2.4	50	0.425	200	1.3	0.034
Pixel	2	4.4	50	0.425	200	1.3	0.059
S0a	3	7.5	58	9.6	240	1.0	0.18
S0b	4	8.5	58	9.6	240	1.0	0.18
S1a	5	31.0	58	9.6	240	0.6	1.4
S1b	6	34.0	58	9.6	240	0.6	1.4
S2	7	64.0	60	9.6	320	1.0	6.5

**OR replace
pixels with**

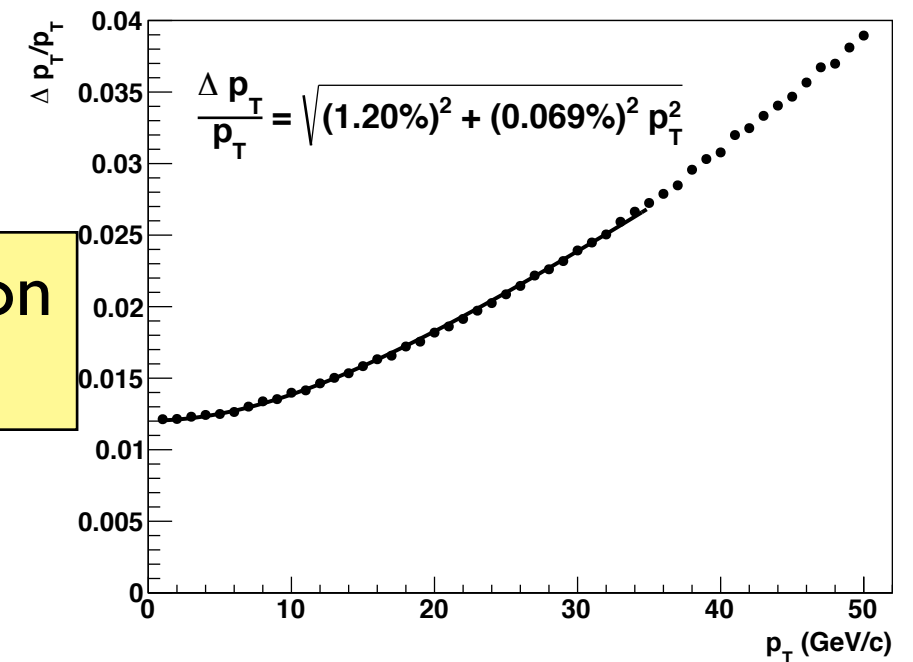
Layer	radius (cm)	pitch (μm)	sensor		total thickness $X_0\%$	length (cm)	area (m^2)
			length (μm)	depth (μm)			
1	2.4	28	28	50	0.3	27	0.041
2	~ 4	28	28	50	0.3	27	~ 0.068
3	$\sim 6-15$	28	28	50	0.3	$\sim 27-39$	$\sim 0.102-0.368$

Results to date - silicon tracker - single particle resolution

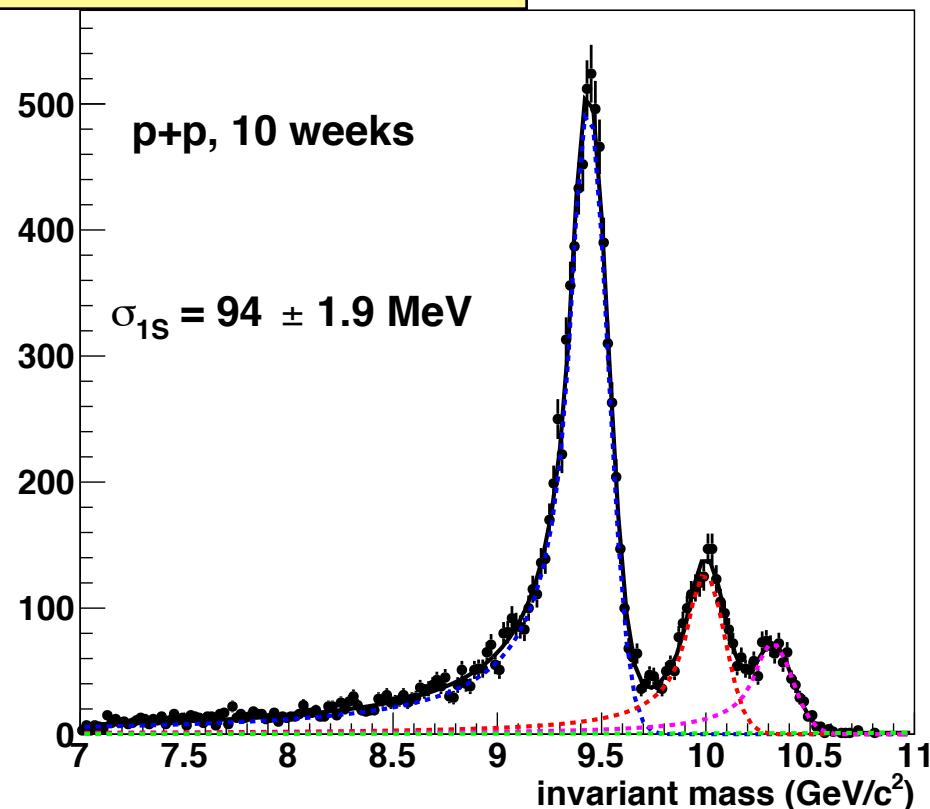
Assume (for the moment) 100% live pixels

- Single pion p_T resolution
- Upsilon mass resolution

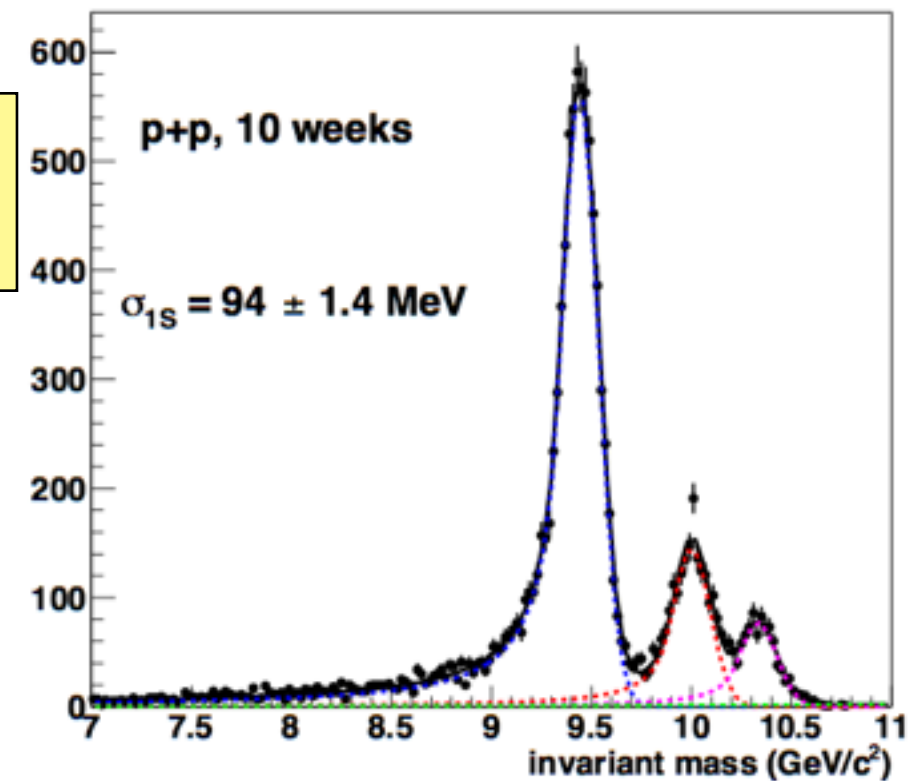
single pion p_T resolution
(either pixel option)



Reused PHENIX
pixels



3 layer MAPS
Pixels



Effect of dead pixels on Upsilon measurement

Do the dead pixels in the reuse option cause problems for the Upsilon measurement?

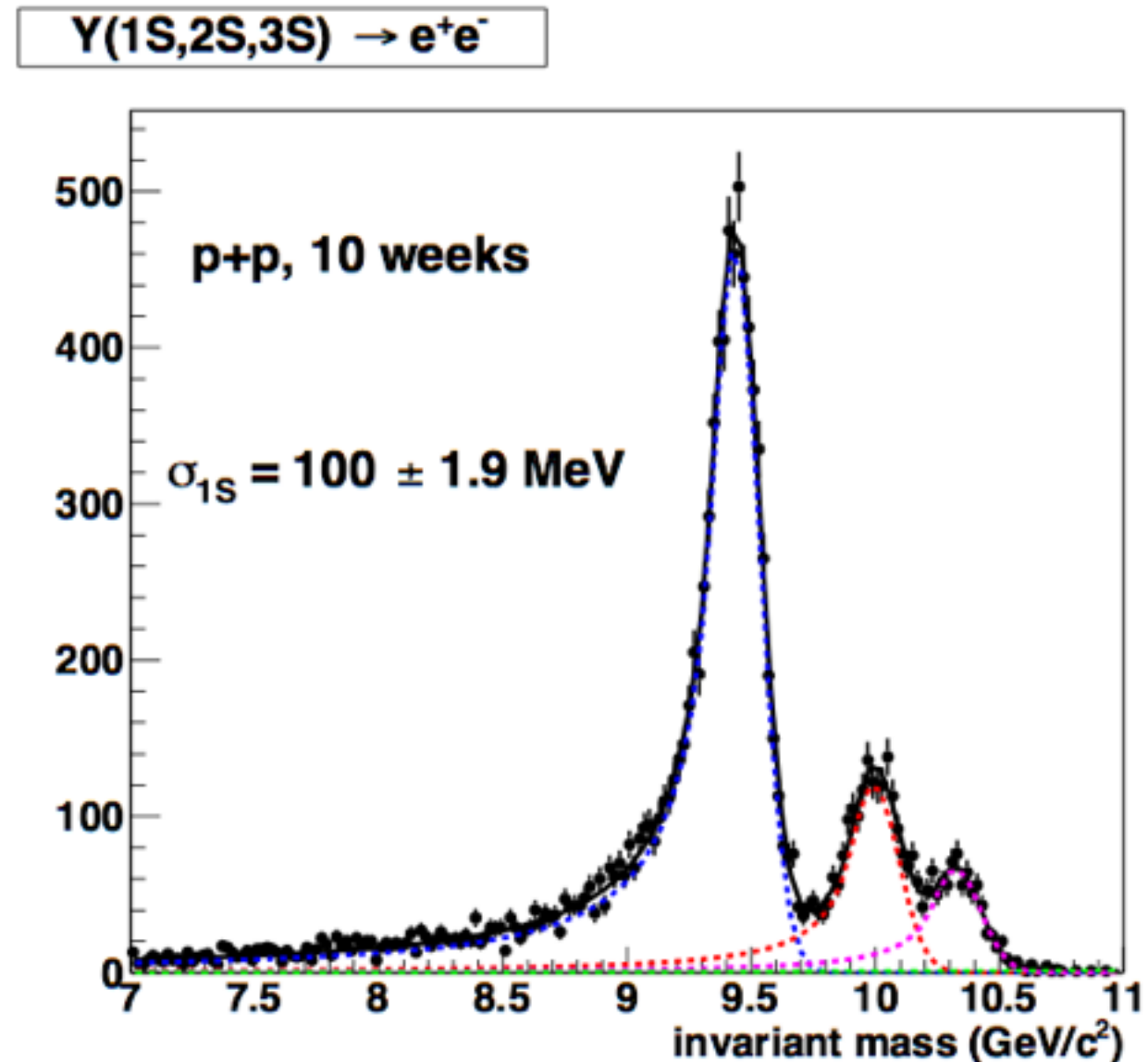
Make layer 1 **92.5%** live

Make pixel layer 2 **72.5%** live

Require hits in only 6 of the 7 layers

- Acceptance increases slightly
- Some loss of resolution
 - likely recover it with tracker setup

Not so bad!



Results to date - TPC - single particle resolution

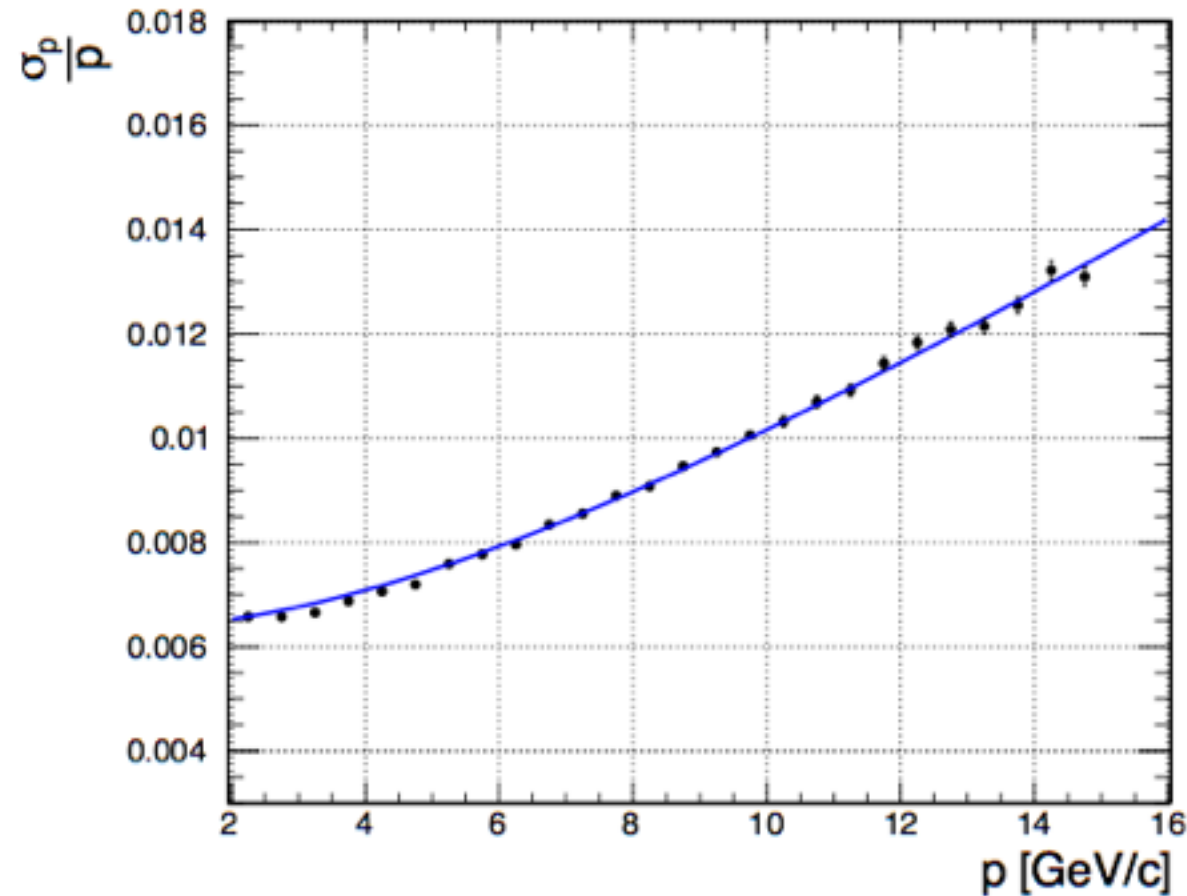
Configuration used for simulations so far:

layer	radius (cm)	Thickness % χ_0	$\frac{\Delta L}{L}$	c_{ms} (mrad)	σ_{ms} (mrad)
VTX 1	2.7	1.3	0.95	1.8	1.7
VTX 2	4.6	1.3	0.92	1.8	1.7
air	15	0.1	0.73	0.03	0.02
Field cage	30	1.0	0.55	1.12	0.5

Assume (for now) pixels are 100% live.

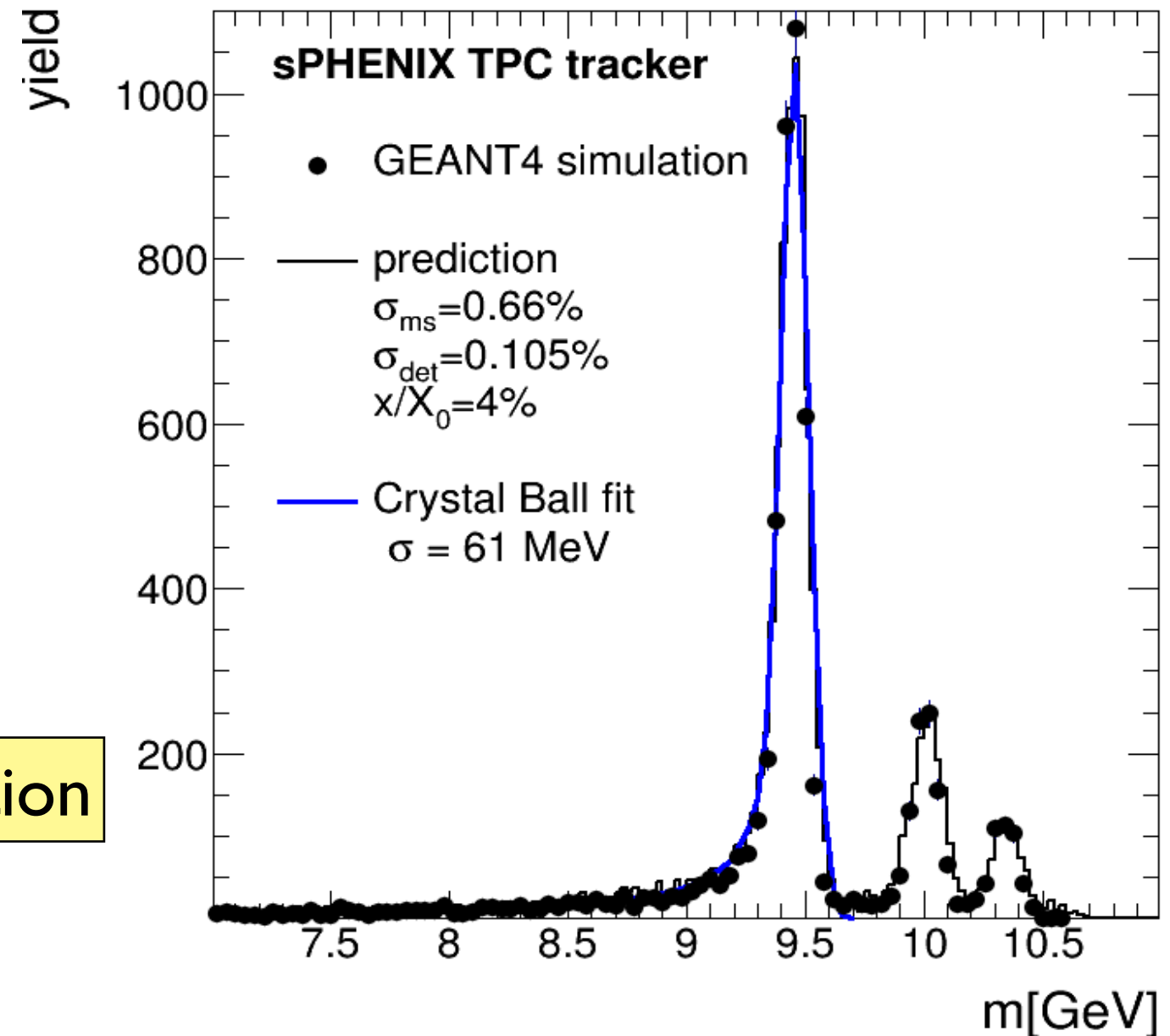
Results to date - TPC - single particle resolution

$0.0 < \eta < 1.0$



Single pion p_T resolution

Single Upsilon mass resolution

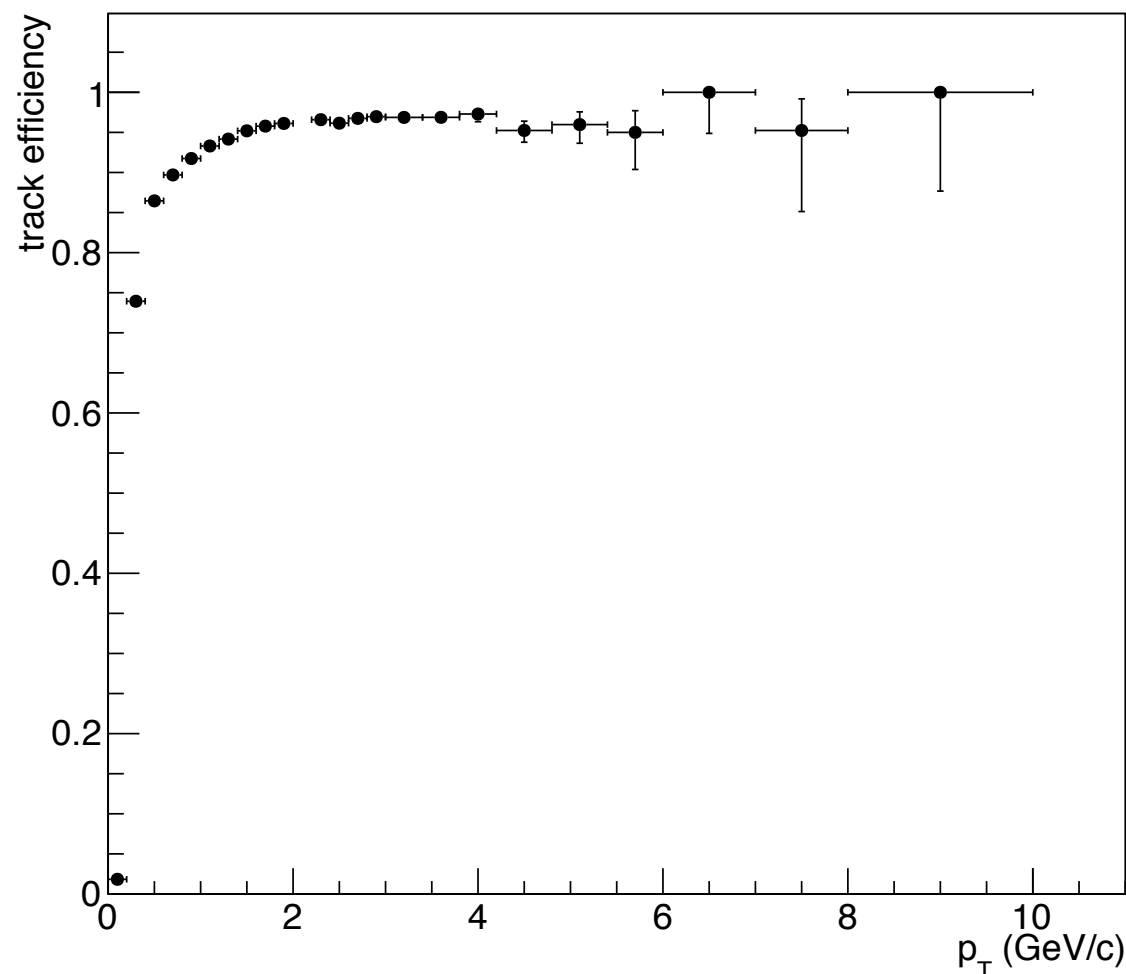


Results to date - silicon tracker - AuAu central

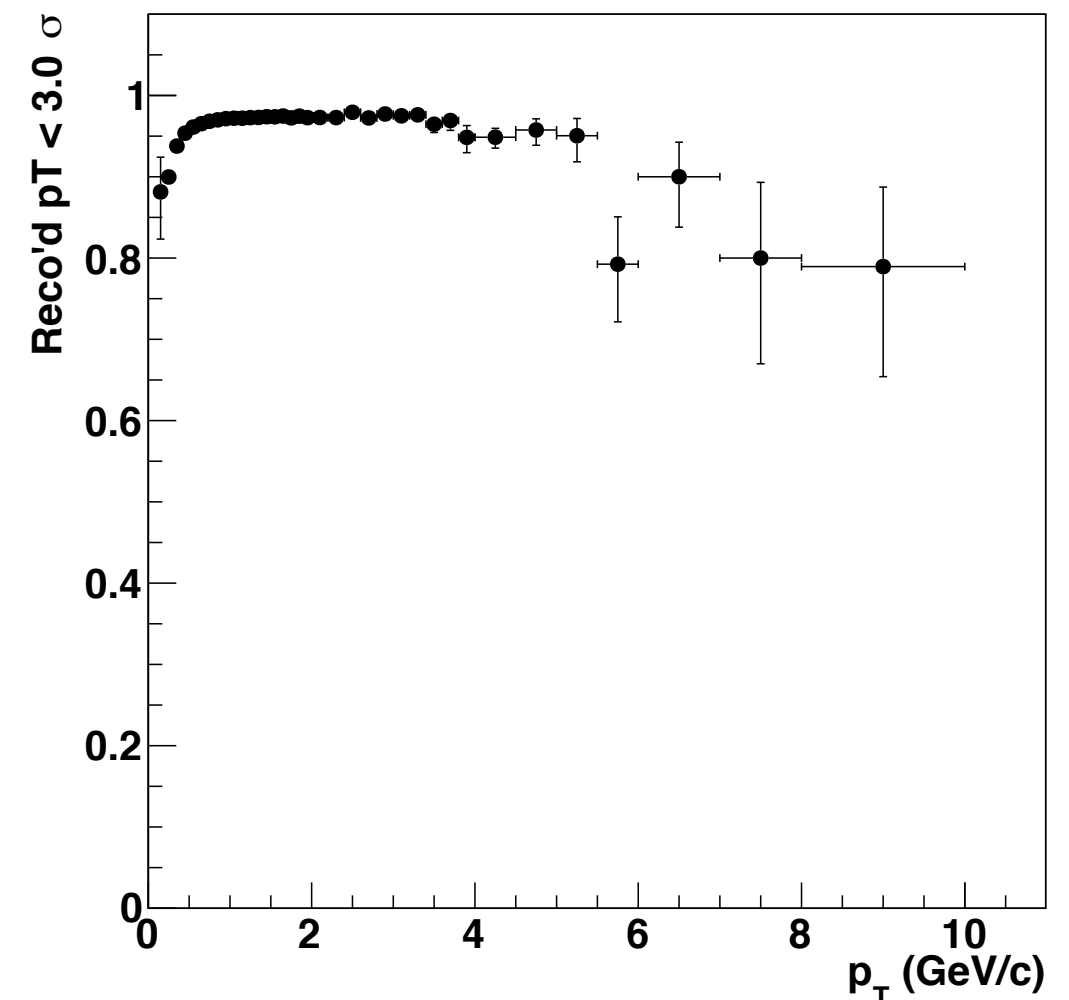
Performance of the silicon strip tracker + **reused pixels** (assume pixels 100% efficient for now) in 5000 central AuAu HIJING events

- Look at track efficiency and track purity

Reconstruction efficiency
all **truth** tracks reconstructed within
 3σ of truth p_T



Track purity
all **reconstructed** tracks within
 3σ of truth p_T

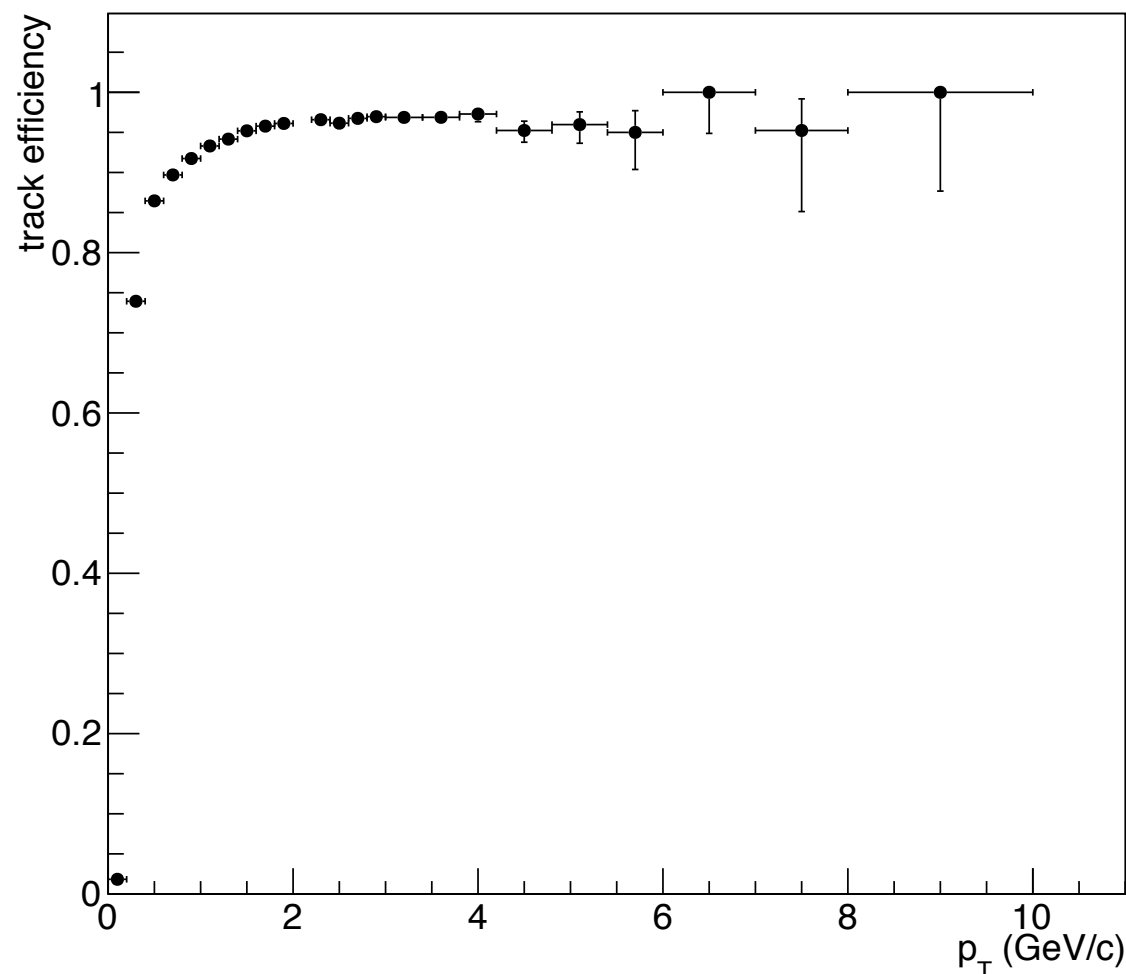


Results to date - silicon tracker - AuAu central

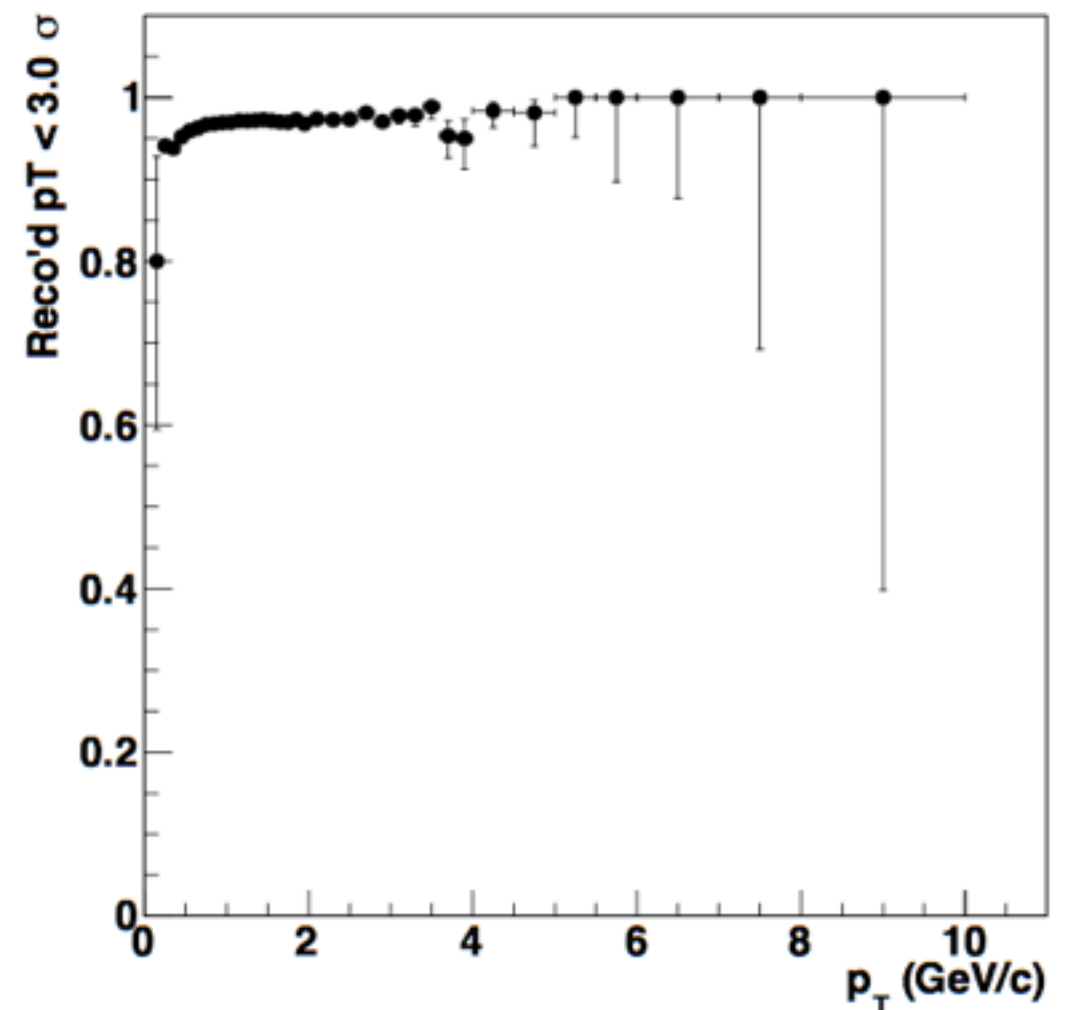
Performance of the silicon strip tracker + **MAPS pixels** in 2000 central AuAu HIJING events

- Look at track efficiency and track purity

Reconstruction efficiency
all **truth** tracks reconstructed within
 3σ of truth p_T



Track purity
all **reconstructed** tracks within
 3σ of truth p_T

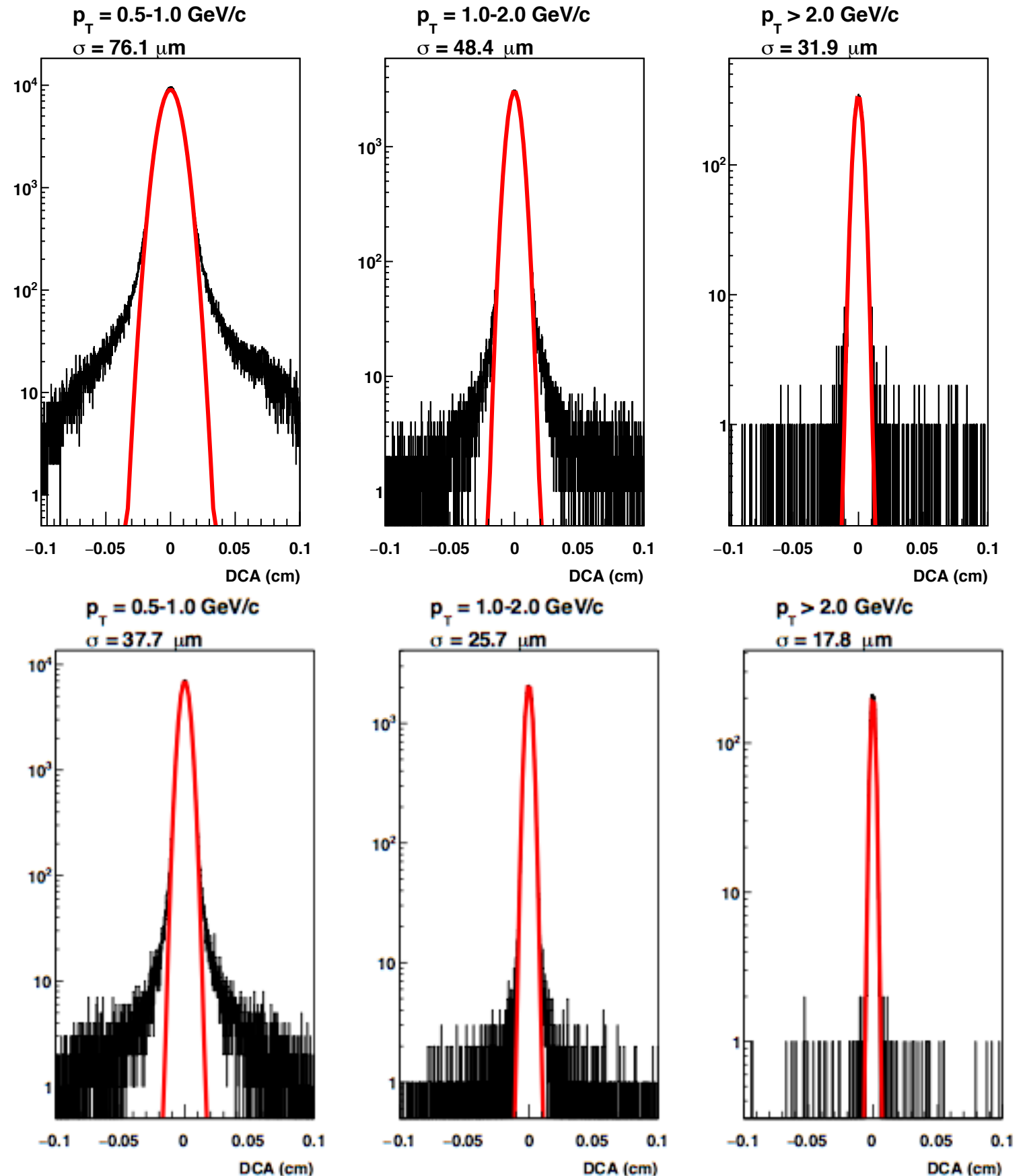


Results to date - silicon tracker - AuAu central

2000 central HIJING AuAu events:

Silicon strip + reused pixels

- Meets our spec of $< 100 \mu\text{m}$
- $46 \mu\text{m}$ for $p_T = 1\text{-}2 \text{ GeV}/c$



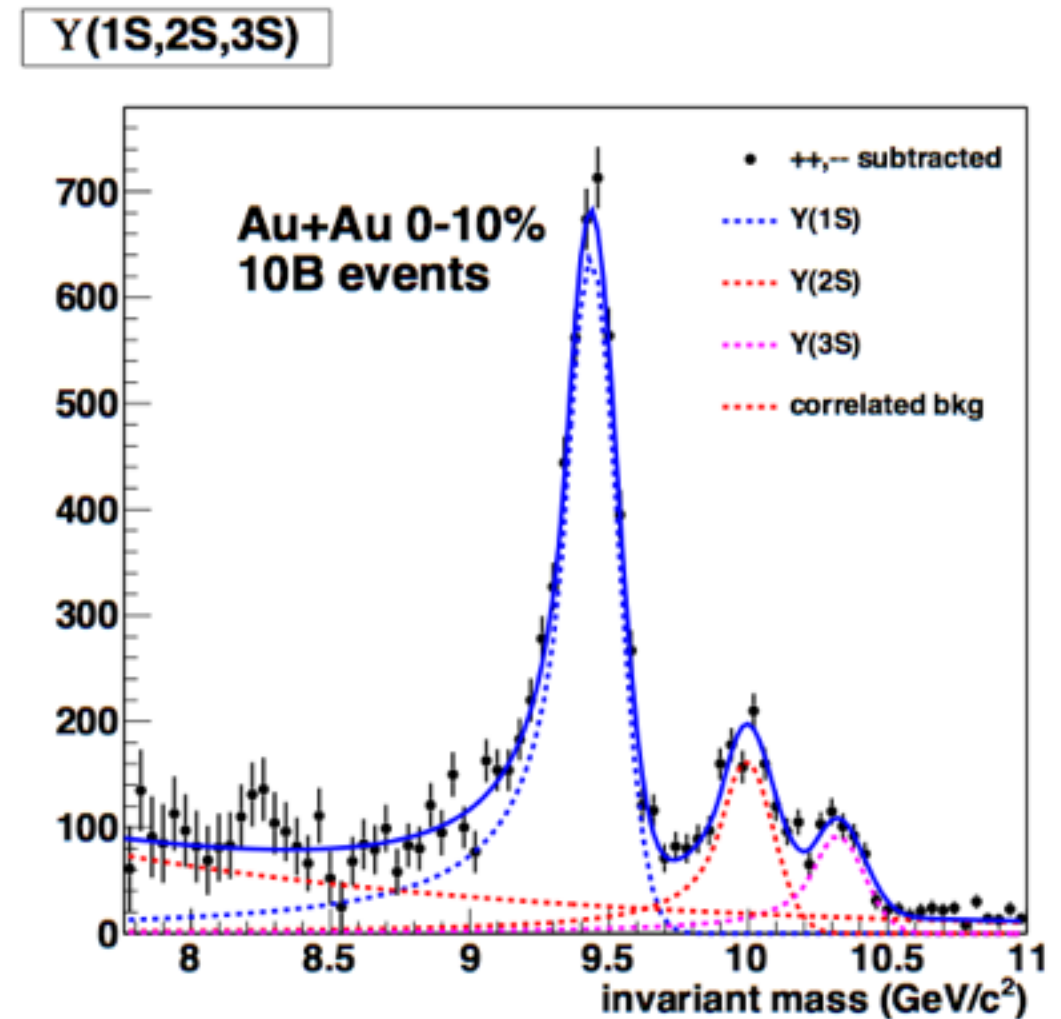
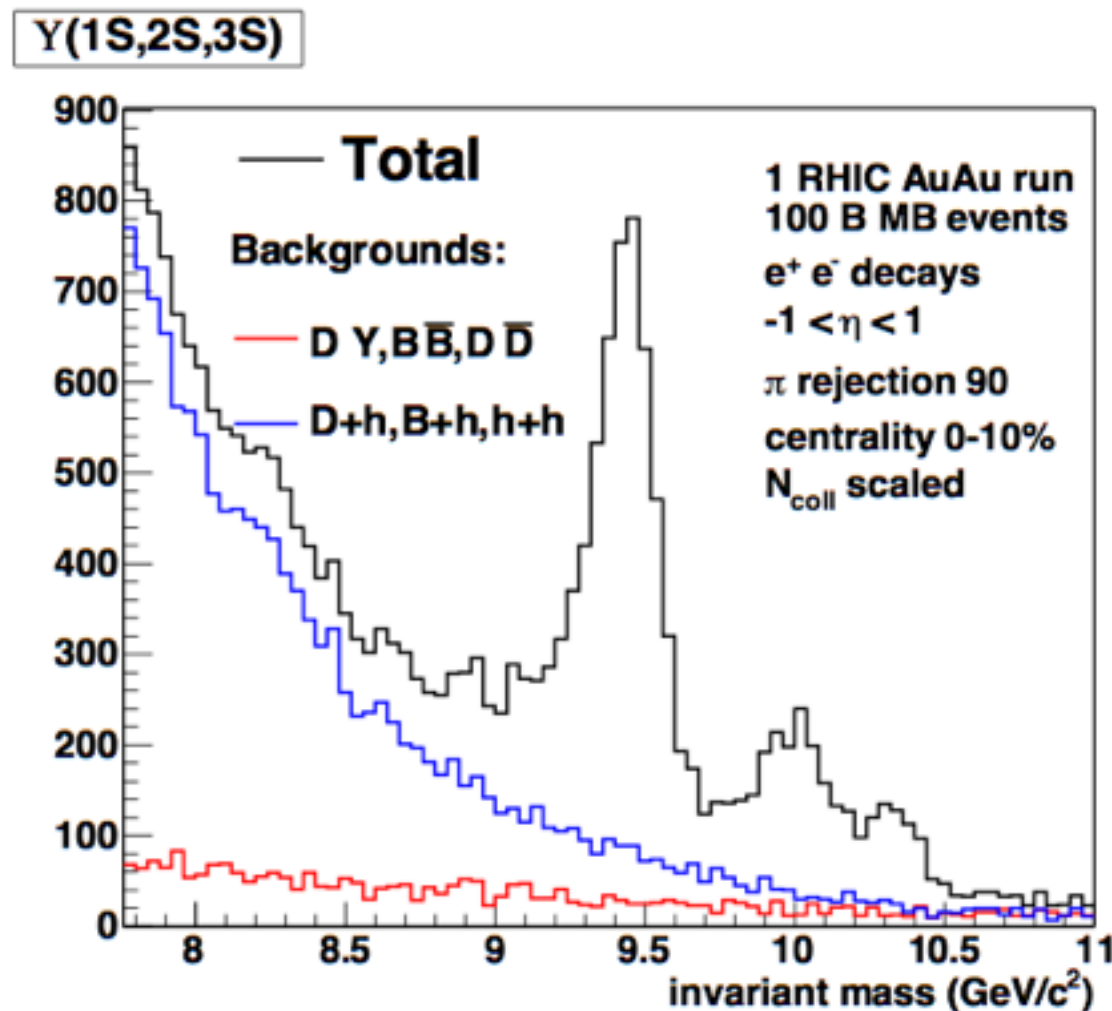
Silicon strip + 3 layer MAPS

- $26 \mu\text{m}$ for $p_T = 1\text{-}2 \text{ GeV}/c$

Results to date - silicon tracker - AuAu central

Fast simulation of background under Upsilon for 0-10% centrality AuAu collisions

- Assumes hadron rejection of 90 (\rightarrow 70% efficiency for single electrons)
- Based on measured pion cross sections in AuAu collisions



Current (ongoing) simulations studies - silicon strip

Simulations work is ongoing to understand the effect of **dead pixels** in the reused pixels option on:

The pattern recognition in central AuAu events

To maintain acceptance, **require** only 1 hit layer in the pixels

- How much does this worsen the track purity?
- Can we live with it, or would we need to add pattern recognition
 - Maybe add stereo layer(s) or shorter, fatter strips?

The b-tagged jet measurement efficiency

We must require hits in **both** pixel layers for b-tagging

- What is the resulting b-tagged jet efficiency?
- Can we live with it?

Current (ongoing) simulations studies - TPC

Starting now to address pattern recognition performance in central AuAu collisions for the TPC + inner tracker

Does the matching of tracks between the TPC (inner radius 40 cm) and the outer layer of the pixels (4.4-6 cm) will work well enough to avoid track efficiency or track purity problems in AuAu events?

- If not, may need an intermediate layer between the pixels and TPC
- Or, possibly, just increase the radius of the 3rd pixel layer

Future simulation pushes

Make realistic ladders in G4 for silicon (strips, reused pixels, MAPS)

- A model was made for the revised MIE strip design (SVX4 chip)
- Waiting for configuration to fully stabilize for FPHX strip version
- Maybe import model of ALICE ITS inner pixels for MAPS?

Realistic simulation of response of TPC gas

- Ionization part is in pretty good shape now
- Need realistic simulation of analog shaper pulse
- Need realistic simulation of the effects of space charge!
- Pattern recognition studies ongoing, needs more work

Assessment of the “cost” to physics of dead areas in reused pixels

Do we need track matching hardware between TPC and inner pixels?

Do we need to add pattern recognition layer(s) in silicon strip tracker?